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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,241	10/22/2003	Yoshifumi Tsunekawa	117207	4913

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EXAMINER	
LEWIS, DAVID LEE	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,241	TSUNEKAWA ET AL.	
	Examiner	Art Unit	
	David L. Lewis	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-15 and 19-21* is/are rejected.

7)☒ Claim(s) *16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :10/22/2003, 2/23, 9/20, ~~11/2/05~~. 11/21/05

✓ ✓

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1-16 and 19-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Shiota et al. (2006/0098132).**

As in claim 1, Shiota et al. teaches of an electro-optical device, **figure 1**,

comprising: data lines extending in a first direction above a substrate, **figure 1 item 13a**;

scanning lines extending in a second direction and intersecting the data lines, **figure 1 item 9**;

pixel electrodes and thin-film transistors arrayed so as to correspond to intersection regions of the data lines and the scanning lines, **figure 1 item 10 and 22, figure 2 item 42**;

capacitors formed at a layer higher than a semiconductor layer of the thin-film transistors and at a layer lower than the pixel electrodes, and electrically connected to pixel potential, **figure 1 item 18**;

and upper light shielding film positioned between the data lines and the pixel electrodes, **figure 1 item 17, paragraph 37**;

the upper light shielding film defining at least the corners of pixel opening regions, **figure 1 item 17**;

and the scanning lines, the data lines, and the capacitors, being formed in the light shielded region, **figure 1 item 17**.

As in claim 2, Shiota et al. teaches of further comprising: a relay layer having light-shielding capabilities, formed of the same film as the upper light shielding film, to electrically connect the thin-film transistors and the pixel electrodes, the shielding film and the relay film defining the pixel opening regions, figure 1 item 15.

As in claim 3, Shiota et al. teaches of the upper shielding film being electrically connected to one of the electrodes forming the capacitors, figure 1 items 15 and 17.

As in claim 4, Shiota et al. teaches of an inter-layer insulating film disposed as a base for the pixel electrodes, figure 1 item 20/21; and contact holds for electric contact with the pixel electrodes being formed on the inter-layer insulating film, figure 1 item 24; and a film including the titanium or a compound thereof being formed on at least the inner face of the contact holes, paragraphs 63-66.

As in claim 5, Shiota et al. teaches of the data lines being formed of the same film with one electrode of the pair of electrodes making up the capacitors, figure 1 item 15, 17.

As in claim 6, Shiota et al. teaches of further comprising: a relay layer, to electrically connect at least one electrode of the pair of electrodes making up the accumulation capacitor with the pixel electrode, figure 1 item 15.

As in claim 7, Shiota et al. teaches of the relay layer being formed of an aluminum film and nitrized film, paragraph 63.

As in claim 8, Shiota et al. teaches of the scanning lines, the data lines, and at least one electrode of the pair of electrodes making up the capacitors, being formed of a light shielding material, figure 1 item 17.

As in claim 9, Shiota et al. teaches of one electrode of the pair of electrodes making up the capacitors making up a part of capacitor lines formed so as to follow the second direction, figure 1 item 15/17; and the capacitor lines being formed of a multi-layer film including a low-resistance film, figure 1 item 15/17.

As in claim 10, Shiota et al. teaches of the capacitor lines having the low-resistance film as an upper layer thereof and a film formed of a light-absorbing layer as a lower layer thereof, figure 1 item 18.

As in claim 11, Shiota et al. teaches of the low-resistance film being formed of aluminum or an aluminum alloy, paragraph 63.

As in claim 12, Shiota et al. teaches of the capacitors, comprising: the dielectric film and an upper electrode and lower electrode holding the dielectric film therebetween, and including a first portion layered following a plane parallel to the surface of the substrate, and a second portion layered following a plane rising from the surface of the substrate, thereby having a stepped cross-sectional shape which is higher at the middle than the portions closer to the edges, figure 1 item 18.

As in claim 13, Shiota et al. teaches of the stepped cross-sectional shape of the capacitors being formed following at least one of the scanning lines and the data lines, figure 1 item 18.

As in claim 14, Shiota et al. teaches of the capacitors, comprising: the dielectric film and an upper electrode and lower electrode holding the dielectric film therebetween, and the dielectric film being formed of a silicon nitride film and a silicon oxide film, figure 1 item 18 (16).

As in claim 15, Shiota et al. teaches of an inter-layer insulating film disposed as a base for the pixel electrodes, further comprising: a part of the layered structure; and the surface of the inter-layer insulating film being subjected to smoothing processing, figure 1 item 20/21.

As in claim 19, Shiota et al. teaches of an electro-optical device, **figure 1,**

comprising: data lines extending in a first direction above a substrate, **figure 1 item 13a**;

scanning lines extending in a second direction and intersecting the data lines, **figure 1 item 9**;

pixel electrodes and thin-film transistors arrayed so as to correspond to intersection regions of the data lines and the scanning lines, **figure 1 item 10 and 22, figure 2 item 42**;

capacitors formed at a layer higher than a semiconductor layer of the thin-film transistors and at a layer lower than the pixel electrodes, and electrically connected to pixel potential, **figure 1 item 18**;

a shielding layer provided between the data lines and the pixel electrodes, **figure 1 item 17, paragraph 37**;

and a lower light shielding film formed at a layer lower than the semiconductor layer of the thin-film transistors, **figure 1 item 6**;

the lower light shielding film defining at least the corners of pixel opening regions, **figure 1 item 6**;

and the scanning lines, the data lines, the capacitors, and the shielding layer, being formed in the light shielded region, **figure 1 item 17**.

As in claim 20, Shiota et al. teaches of the shielding layer having light shielding capabilities, figure 1 item 17, paragraph 37.

As in claim 21, Shiota et al. teaches of an electronic apparatus, having an electro-optical device, figure 1,

comprising: data lines extending in a first direction above a substrate, **figure 1 item 13a**;

scanning lines extending in a second direction and intersecting the data lines, **figure 1 item 9**;

pixel electrodes and thin-film transistors arrayed so as to correspond to intersection regions of the data lines and the scanning lines, **figure 1 item 10 and 22, figure 2 item 42**;

capacitors formed at a layer higher than a semiconductor layer of the thin-film transistors and at a layer lower than the pixel electrodes, and electrically connected to pixel potential, **figure 1 item 18**;

and upper light shielding film positioned between the data lines and the pixel electrodes, **figure 1 item 17, paragraph 37**;

the upper light shielding film defining at least the corners of pixel opening regions, **figure 1 item 17, paragraph 37**;

and the scanning lines, the data lines, and the capacitors, being formed in the light shielded region, **figure 1 item 17, paragraph 37**.

Claim Objections

2. Claims 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. 6831297, 6219118, 2005/0099557, 2001/0002144, 2002/0071072.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **David L. Lewis** whose telephone number is **(571) 272-7673**. The examiner can normally be reached on MT and THF from 8 to 5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached on **(571) 272-7681**. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571)-273-8300.

5. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: David L. Lewis
January 6, 2007